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### A post-compiler approach to scratchpad mapping of code

F Angiolini, F Menichelli, A Ferrero, L Benini, M ... - Proceedings of the 2004 international conference on ..., 2004 - portal.acm.org

... to apply some of the above proposals as a post-compiler pass, fetching ... 3.3 Simulation Platform Our work builds upon a fully parametric multiprocessor platform ... Cited by 1 - Web Search - portal.acm.org

# <u>Dictionary Based Code Compression for Variable Length Instruction Encodings</u>

D Das, R Kumar, PP Chakrabarti - Proceedings of the 18th International Conference on VLSI ..., 2005 doi.ieeecomputersociety.org

... In section 5 we present our simulation results for the algorithm applied ... can be broadly categorized into compiler optimizations and post compiler optimizations ... Web Search - ieeexplore.ieee.org - ieeexplore.ieee.org - portal.acm.org

## SCISM IA-32 Binary Translator

E Koukourechkov, N Grozdanov, G Gaydadjiev, S ... - stw.nl

... the compounding facility may be a software facility - in the form of a post compiler

[5] or ... clear steps are to be performed as a part of the simulation process ...

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#### A compiler directed framework for parallel compositional systems

J Mukheriee, N Ramakrishnan, JD Arthur, V ... - Master's thesis, Department of Computer Science, Virginia ..., 2002 - scholar.lib.vt.edu

... Our post compiler analysis automatically determines the necessary state that is

to be saved and restored and presents a simple interface to this functionality. ...

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### rest Latency-directed multithreaded computation and its architectural support

X Fan - 1994 - tams-www.informatik.uni-hamburg.de

... The simulation results are presented. Finally, some ...

83 4.4.2 Simulation Results : : : : 85 ...

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# A scalable compound instruction set machine

S Vassiliadis, B Blaner - research.ibm.com

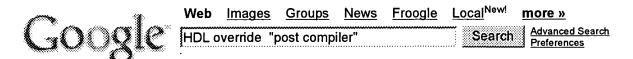
Page 1. SCISM: A scalable compound instruction set machine by S. Vassiliadis

B. Blaner I?. J. Eickemeyer In this paper we describe ...

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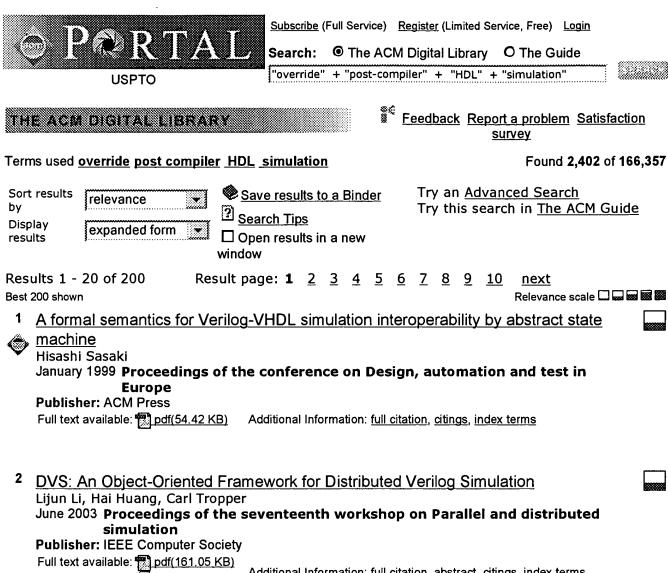
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There is a wide-spread usage of hardware design languages(HDL) to speed up the time-

There is a wide-spread usage of hardware design languages(HDL) to speed up the time-to-market for the designof modern digital systems. Verification engineers can simulatehardware in order to verify its performance and correctnesswith help of an HDL. However, simulation can'tkeep pace with the growth in size and complexity of circuitsand has become a bottleneck of the design process. DistributedHDL simulation on a cluster of workstations hasthe potential to provide a cost-effective solution to th ...

3 Regression-based RTL power modeling

Alessandro Bogliolo, Luca Benini, Giovanni De Micheli
July 2000 ACM Transactions on Design Automation of Electronic Systems (TODAES),

Valume 5 Issue 3

Publisher: ACM Press

Full text available: pdf(391.65 KB)

Additional Information: full citation, abstract, references, citings, index terms

Register-transfer level (RTL) power estimation is a key feature for synthesis-based design flows. The main challenge in establishing a sound RTL power estimation methodology is the construction of accurate, yet efficient, models of the power dissipation of functional macros. Such models should be automatically built, and should produce reliable average power estimates. In this paper we propose a general methodology for building and tuning RTL power models. We address both hard macros (presy ...

Keywords: RTL design, RTL power modeling, adaptive characterization, functional macros, regression models

# Automatic Formal Verification of Fused-Multiply-Add FPUs

Christian Jacobi, Kai Weber, Viresh Paruthi, Jason Baumgartner

March 2005 Proceedings of the conference on Design, Automation and Test in Europe - Volume 2

**Publisher: IEEE Computer Society** 

Full text available: pdf(241.82 KB) Additional Information: full citation, abstract

In this paper we describe a fully-automated methodology for formal verification of fusedmultiply-add floating point units (FPUs). Our methodology verifies an implementation FPU against a simple reference model derived from the processor's architectural specification, which may include all aspects of the IEEE specification including denormal operands and exceptions. Our strategy uses a combination of BDD- and SAT-based symbolic simulation. To make this verification task tractable, we use a combi ...

# 5 Teaching computer organization and architecture using SystemC

**Ed Harcourt** 

December 2005 Journal of Computing Sciences in Colleges, Volume 21 Issue 2

Publisher: Consortium for Computing Sciences in Colleges

Full text available: pdf(346.75 KB) Additional Information: full citation, abstract, references

Hardware simulation is often used in courses that contain a hardware component. We describe and introduce SystemC, a C++ library for designing, simulating, and analyzing digital systems. We compare and contrast the strengths and weaknesses of SystemC to other technologies used in hardware courses such as breadboards and other simulation technologies including schematic capture and traditional hardware description languages Verilog and VHDL. We ascertained the strengths and weaknesses of using Sy ...

# Adaptive least mean square behavioral power modeling

A. Bogliolo, L. Benini, G. De Micheli

March 1997 Proceedings of the 1997 European conference on Design and Test

**Publisher: IEEE Computer Society** 

Full text available: pdf(891.01 KB)

Additional Information: full citation, abstract, citings

In this work we propose an effective solution to the main challenges of behavioral power modeling: the generation of models for the power dissipation of technology-independent soft macros and the strong dependence of power from input pattern statistics. Our methodology is based on a fast characterization performed by simulating the gate-level implementation of instances of soft macros within the behavioral description of the complete design. Once characterization has been completed, the backanno ...

**Keywords:** adaptive least mean square behavioral power model, design, gate-level power simulation, integrated circuit modelling, pattern statistics, power dissipation, soft macro, synthesis

# Functional verification methodology for the PowerPC 604 microprocessor

James Monaco, David Holloway, Rajesh Raina

June 1996 Proceedings of the 33rd annual conference on Design automation

Publisher: ACM Press

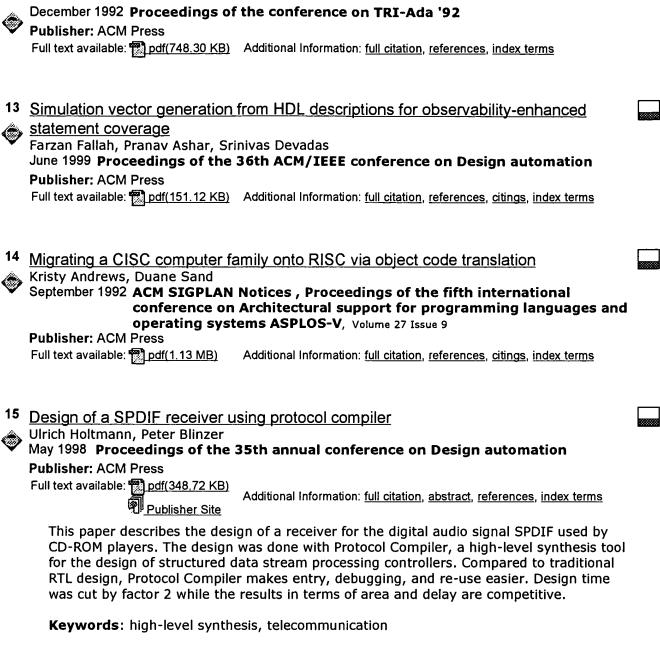
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full citation, references, citings, index terms

CAD: ARCS: an architectural level communication driven simulator Dave Nellans, Vamshi Krishna Kadaru, Erik Brunvand April 2004 Proceedings of the 14th ACM Great Lakes symposium on VLSI Publisher: ACM Press Full text available: pdf(138.92 KB) Additional Information: full citation, abstract, references, index terms Simulators for digital systems operate at a variety of levels of abstraction varying from detailed analog and switch level modeling of the transistor to cycle based descriptions of entire systems. We propose an even higher level simulator, called ARCS, based on the abstraction of an asynchronous communication event rather than of a clock cycle. Modeling systems at this level allows architectural level exploration of the design space before cycle-level details are available, and also allows the s ... **Keywords:** Java, architectural simulation, asynchronous communication 9 (Special session) invited talks: c-based design examples: Using C based logic synthesis to bridge the productivity gap Chris Sullivan, Alex Wilson, Stephen Chappell January 2004 Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04, Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 Publisher: IEEE Press, IEEE Press Full text available: pdf(375.82 KB) Additional Information: full citation, abstract Publisher Site Digital circuits from software designs and formal executable specifications can be automatically synthesized using hardware compilation or 'C based logic synthesis'. Designs can be verified using that same formal specification and coupled with the increasing deployment of higher-level C based languages and IP reuse in hardware design and system codesign, C based logic synthesis is enabling new methodologies and levels of designer productivity. In this paper we discuss the rationale for such a sy ... 10 Design and use of a system-level specification and verification methodology M. M. Kamal Hashmi, Alistair C. Bruce December 1995 Proceedings of the conference on European design automation **Publisher: IEEE Computer Society Press** Full text available: 📆 pdf(624.83 KB) Additional Information: full citation, references, citings, index terms 11 RuleBase: an industry-oriented formal verification tool Ilan Beer, Shoham Ben-David, Cindy Eisner, Avner Landver June 1996 Proceedings of the 33rd annual conference on Design automation Publisher: ACM Press Full text available: pdf(75.02 KB) Additional Information: full citation, references, citings, index terms When hardware becomes software: designing a safety-critical system with Ada James Hummer, Loïc Briand



16 Synthesis for Low Power: Dynamic modeling of inter-instruction effects for execution

time estimation

G. Beltrame, C. Brandolese, W. Fornaciari, F. Salice, D. Sciuto, V. Trianni

September 2001 Proceedings of the 14th international symposium on Systems synthesis

Publisher: ACM Press

Full text available: pdf(234.84 KB) Additional Information: full citation, abstract, references, index terms

The market for embedded applications is facing a growing interest in power consumption issues: this work is intended to provide a new model to estimate software-level power consumption of 32-bit microprocessors. This model extends previous ones by considering dynamic inter-instruction effects that take place during code execution, providing a static means to characterize their energy consumption. The model is formally sound: it is conceived for a generic architecture and it has been preliminary ...

17	Defeat estanted universal level facult aim vilation of digital average on a phin visitar LIDI	
	<u>Defect-oriented mixed-level fault simulation of digital systems-on-a-chip using HDL</u> M. B. Santos, J. P. Teixeira	
V	January 1999 Proceedings of the conference on Design, automation and test in	
	Europe Publisher: ACM Press	
	Full text available: pdf(57.77 KB) Additional Information: full citation, citings, index terms	
40		
18	Generation of the HDL-A-Model of a Micromembrane from Its Finite-Element-	********
	<u>Description</u> Klaus Hofmann, Manfred Glesner, Nicu Sebe, A. Manolescu, Santiago Marco, Josep Samitier,	
	Jean-Michel Karam, Bernard Courtois	
	March 1997 Proceedings of the 1997 European conference on Design and Test Publisher: IEEE Computer Society	
	Full text available: 😭 pdf(574.37 KB)	
	Additional Information: <u>full citation</u> , <u>abstract</u>	
	A CAD tool for the automated generation of behavioral models in HDL-A is presented. This CAD tool has been implemented in the frame of a project for the automatic modeling of microsystem components for the co-simulation with VHDL or Spice-models. Starting from the finite-element-description of a microcomponent a nonlinear behavioral HDL-A-model is generated by successively adding or deleting effects to the HDL-A-model according to	
	the observed differences between the two models. Using the exampl	
	<b>Keywords</b> : logic CAD, HDL-A-model, micromembrane, finite-element-description, CAD tool, automated generation, behavioral models, FEM, microsystem components, automatic modeling, cosimulation, VHDL-models, Spice-models	
10		
19	Behavioral synthesis methodology for HDL-based specification and validation  D. Knapp, T. Ly, D. MacMillen, R. Miller	
<b>~</b>	January 1995 Proceedings of the 32nd ACM/IEEE conference on Design automation	
	Publisher: ACM Press	
	Full text available: pdf(51.94 KB) Additional Information: full citation, references, citings, index terms	
20	Advances in hardware/software co-simulation techniques: RTOS-centric	
۱	hardware/software cosimulator for embedded system design	
	Shinya Honda, Takayuki Wakabayashi, Hiroyuki Tomiyama, Hiroaki Takada September 2004 Proceedings of the 2nd IEEE/ACM/IFIP international conference on	
	Hardware/software codesign and system synthesis	
	Publisher: ACM Press Full text available: pdf(510.21 KB) Additional Information: full citation, abstract, references, index terms	
	This paper presents an RTOS-centric hardware/software cosimulator which we have developed for embedded system design. One of the most remarkable features in our cosimulator is that it has a complete simulation model of an RTOS which is widely used in industry, so that application tasks including RTOS service calls are natively executed on a host computer. Our cosimulator also features cosimulation with functional simulation	
	models of hardware written in C/C++ and cosimulation with HDL simulators	
	Keywords: RTOS, cosimulation, embedded Systems	

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